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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Glen Fox, Fan Chu, Brian Eastep, Tomohiro Takamatsu, Ko Nakamura, and Yoshimasa Horii

Serial No. 09/742,204

Filed: December 20, 2000

For: PROCESS FOR PRODUCING HIGH QUALITY PZT FILMS FOR FERROELECTRIC MEMORY INTEGRATED CIRCUITS

Group Art Unit: 2811

Examiner:

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

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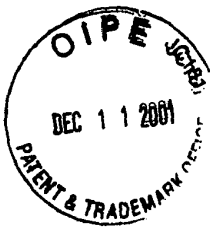
relating to the above application, were deposited as "Express Mail", Mailing Label No. EV035490605US with the United States Postal Service, addressed to The Assistant Commissioner for Patents, Washington, D.C., 20231, on 11 December 2001

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Peter J. Meza
Peter J. Meza, Reg. No. 32,920
HOGAN & HARTSON LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5906 Tel
(303) 899-7333 Fax



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FILMS FOR FERROELECTRIC MEMORY INTEGRATED
CIRCUITS

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Art Unit: 2811

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified patent application as follows:

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 7, line 1, with the following:

A) Figure 3 is a process flowchart illustrating an alternative process wherein
the top electrode layer is deposited following a first RTA anneal, and a second
RTA anneal is performed after etching of the PZT;

Please replace the paragraph beginning at page 7, line 5, with the following:

AB Figure 4 is a process flowchart illustrating an alternative process wherein
the top electrode layer is deposited following a first RTA anneal, and a second
RTA anneal is performed after etching of the PZT and deposition of an
encapsulation layer; and